B2 (contd)

the output thereof is a value in the vicinity of 180° on the contrary, as shown in Fig. 2.--

Please amend the paragraph beginning on page 16, line 20 by rewriting same to read as follows:

--Moreover, though the first position detection head 15 and the second position detection head 16 are arranged so as to effect a phase shift by 1/4 wavelength in the detected signal, these may be arranged so as to effect the phase shift not only by 1/4 wavelength but also by other phase value, since with the position detection apparatus 1, a position in one period of the position signal has only to be specified by an angle, from two signals detected by the polar conversion section 6 described later.--

B3

Please amend the paragraph beginning on page 43, line 20 by rewriting same to read as follows:

--The response limiting section 10 has a first subtractor 70, an absolute value conversion circuit 71, a second subtractor 72, a multiplexer 73, a through rate generating circuit 74, a comparator 75, an absolute value inverse circuit 76, an adder 77 and a latch 78.--

B4

Please amend the paragraph beginning on page 54, line 16 by rewriting same to read as follows:

--As shown in Fig. 31, 24-bit in-quadrant division unit address PDL (PDL0-PDL23) are output from the first multiplier 81. From the second multiplier 82, 4-bit correction address PC ((PH14, PH15)*(DivL0, DivL1) = PC14, PC15, PC16, PC16) is

B5